

### TO-252-3L 650V SiC Schottky Diode EL-SAS00465JA



$V_{RRM}$	=	650	V
$Q_c$	=	6.4	nC
$I_F$	=	4	A
$V_F$	=	1.4	V

#### Features

- Low Forward Voltage
- Ultra-Fast Switching
- Zero Reverse Recovery Current
- High-Frequency Operation and increased power density
- High Surge Current Capability
- Pb-free Lead, Halogen Free, ROHS Compliant

#### Benefits

- Improve System Efficiency
- Reduction of Heat Sink Requirement
- Essentially No Switching Losses
- Parallel Devices Without Thermal Runaway

#### Applications

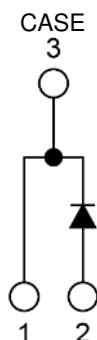
- Solar inverter/Motor Drivers/Data Center
- Boost Diodes in PFC or DC/DC Stages
- AC/DC Converters

#### Key Performance Parameters

Symbol	$V_{RRM}$	$I_F$	$I_{FSM}$	$Q_c$	$T_{J,max}$
Value	650V	4A	12A	6.4nC	175°C
Condition	$T_c@25^\circ\text{C}$		$t_p=10\text{ms}$ $T_c@25^\circ\text{C}$ Sine half wave	$V_R = 400 \text{ V}, T_j = 25^\circ\text{C}$ $Q_c = \int_0^{V_R} C(V) dV$	-

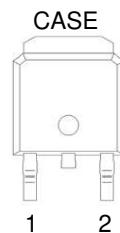


#### Schematic



#### Pin Configuration

1. Cathode
2. Anode
- CASE: Cathode



## Maximum Ratings

Parameter	Symbol	Value	Unit	Test condition
Repetitive Peak Reverse Voltage	$V_{RRM}$	650	V	
Surge Peak Reverse Voltage	$V_{RSM}$	650	V	
DC Blocking Voltage	$V_R$	650	V	
Continuous Forward Current	$I_F^{*1}$	4	A	
Surge non-repetitive forward current	$I_{FSM}$	12	A	$t_p = 10\text{ms}$ Sine half wave
Total power dissipation	$P_D$	25	W	
Junction temperature	$T_J$	175	°C	
Storage temperature	$T_{STG}$	-55 / +175	°C	

\*1 Limited by maximum  $T_A$  and for Max.  $R_{thJC}$ .

## Thermal Characteristics (Measured conformable to JESD51-14.)

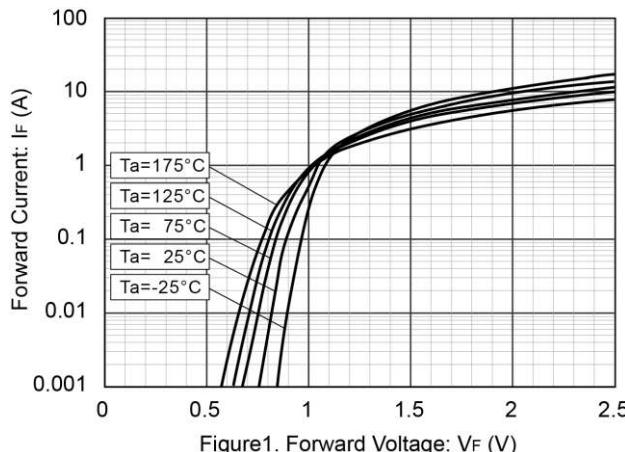
Parameter	Symbol	Value		Unit
		Typ	Max	
Thermal Resistance from Junction to Case	$R_{thJC}$	5.9	-	°C/W

## Electrical Characteristics

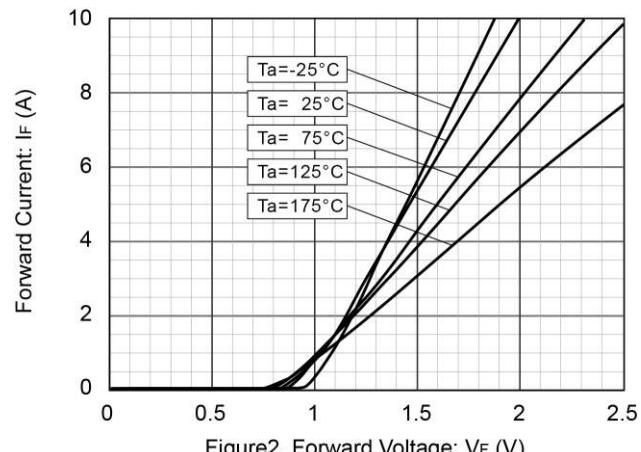
Parameter	Symbol	Values			Unit	Test condition
		Min.	Typ.	Max.		
DC blocking voltage	$V_{DC}$	650	-	-	V	$T_J = 25^\circ C, I_R = 40\mu A$
Forward voltage	$V_F$	-	1.4	1.75	V	$I_F = 4A, T_J = 25^\circ C$
			1.8	-		$I_F = 4A, T_J = 175^\circ C$
Reverse current	$I_R$	-	1	25	$\mu A$	$V_R = 520V, T_J = 25^\circ C$
			1.8	-		$V_R = 520V, T_J = 175^\circ C$
Total capacitance	C	-	100	-	$pF$	$V_R = 1V, f = 1MHz$ $T_J = 25^\circ C$
			12			$V_R = 200V, f = 1MHz$ $T_J = 25^\circ C$
			10			$V_R = 400V, f = 1MHz$ $T_J = 25^\circ C$
Capacitance Stored Energy	$E_C$	-	1.0	-	$\mu J$	$V_R = 400V$
Total capacitive charge	$Q_C$	-	6.4	-	$nC$	$V_R = 400V, T_J = 25^\circ C$ $Q_C = \int_0^{V_R} C(V) dV$

## Typical Performance

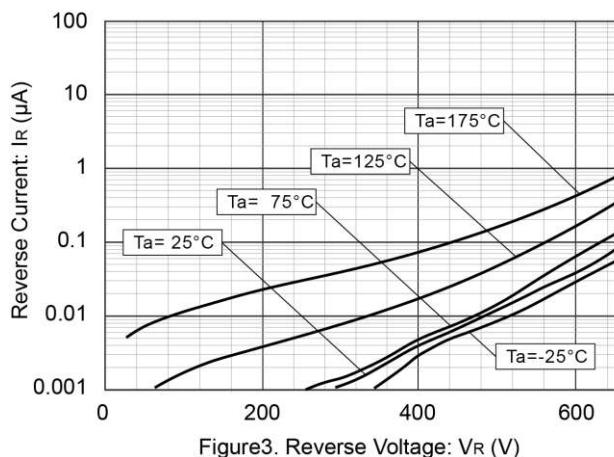
### $V_F$ - $I_F$ Characteristics



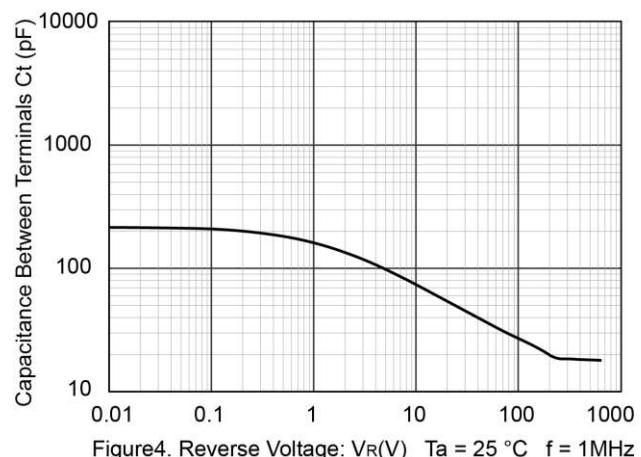
### $V_F$ - $I_F$ Characteristics



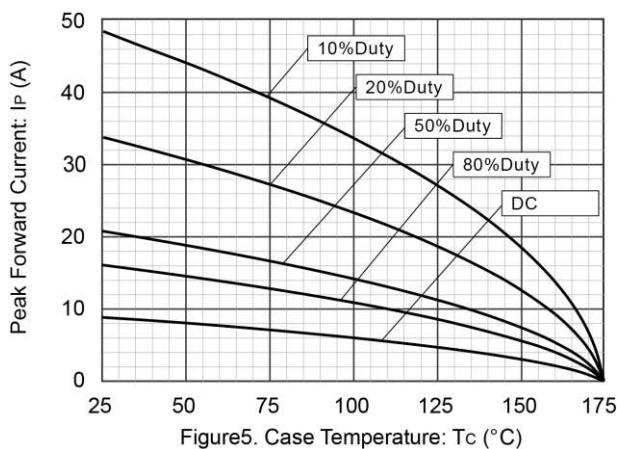
### $V_R$ - $I_R$ Characteristics



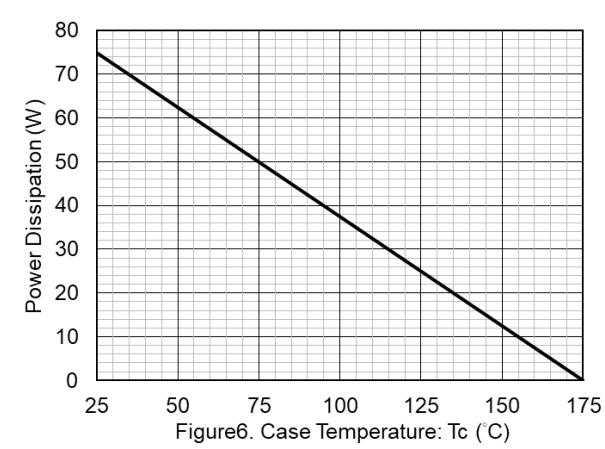
### $V_R$ - $C_t$ Characteristics



### Maximum $I_p$ – $T_c$ Characteristics



### Power Dissipation



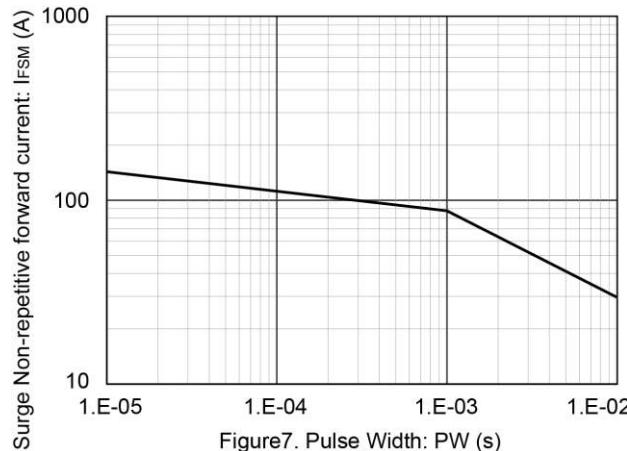
**I<sub>FSM</sub> – P<sub>W</sub> Characteristics**

Figure 7. Pulse Width: PW (s)

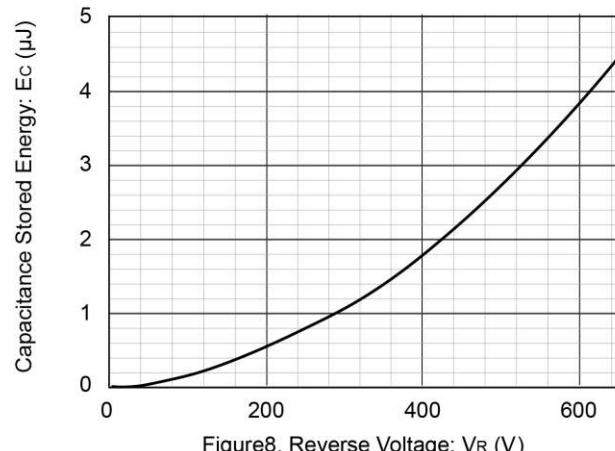
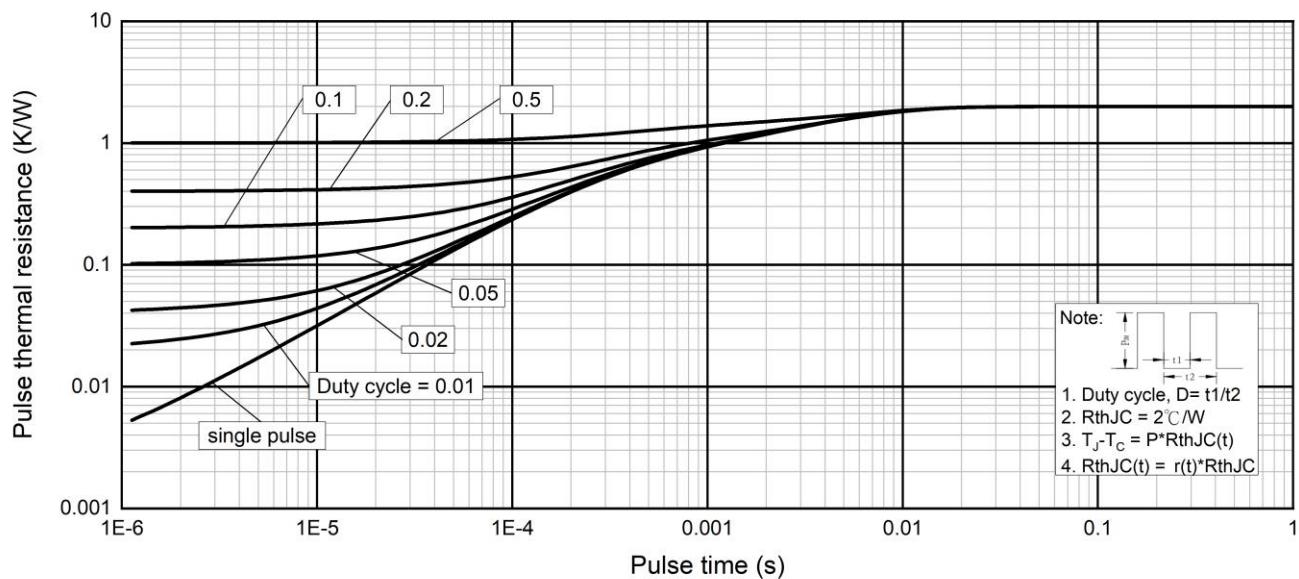
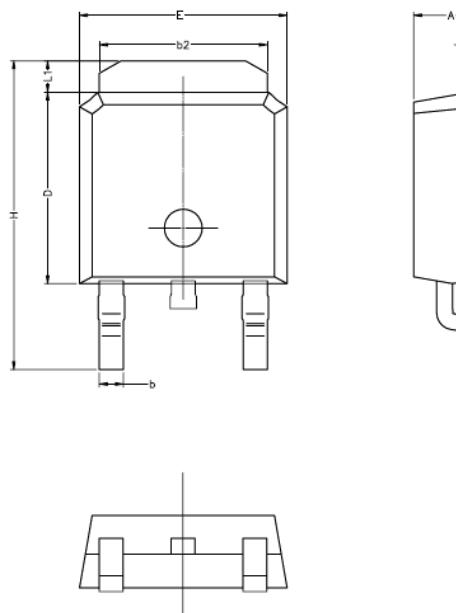
**E<sub>C</sub>-V<sub>R</sub> Characteristics**

Figure 8. Reverse Voltage: VR (V)

**Typical Transient Thermal Resistance vs. Pulse Width**

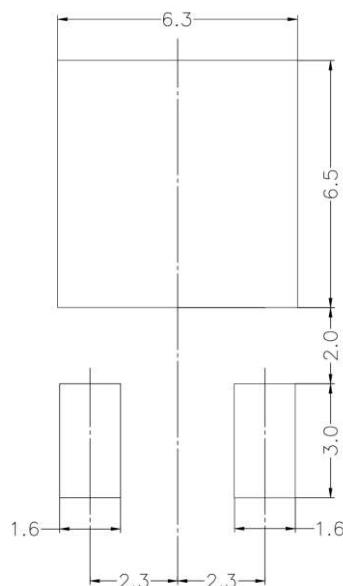
## Package Outlines



Unit : mm

DIM	MILLIMETERS		
	MIN	TYP.	MAX
A	2.10	2.30	2.50
b	0.51	0.76	1.01
b1	0.59	0.84	1.09
b2	5.08	5.33	5.58
c	0.26	0.51	0.76
D	5.90	6.10	6.30
D1	4.98	5.23	5.48
E	6.40	6.60	6.80
E1	4.58	4.83	5.08
e1	2.28BSC.		
H	9.59	9.84	10.09
L	1.27	1.52	1.77
L1	0.75	1.00	1.25

## Recommended pad layout for surface mount leadform



Unit : mm

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