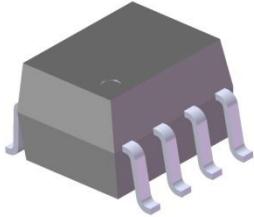


DATASHEET

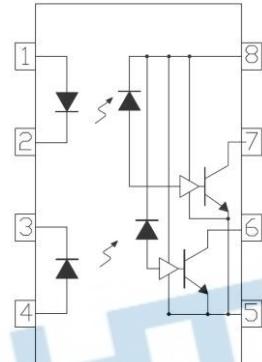
8 PIN SOP DUAL CHANNEL HIGH SPEED 10MBit/s LOGIC GATE PHOTOCOUPLER EL063X Series



Features

- Compliance Halogen Free .
(Br <900 ppm ,Cl <900 ppm , Br+Cl < 1500 ppm)
- High speed 10Mbit/s
- 10kV/μs min. common mode transient immunity (EL0631)
- Guaranteed performance from -40 to 85°C
- Wide operating temperature range of -40°C to 100°C
- Logic gate output
- High isolation voltage between input and output (Viso=3750 V rms)
- Compliance with EU REACH
- Pb free and RoHS compliant
- UL and cUL approved(No. E214129)
- VDE approved (No.40028116)
- SEMKO approved
- NEMKO approved
- DEMKO approved
- FIMKO approved

Schematic



Pin Configuration

1. Anode
2. Cathode
3. Cathode
4. Anode
5. Gnd
6. Vout 2
7. Vout 1
8. Vcc

Description

The EL0630 and EL0631 are dual channel devices each consists of an infrared emitting diode optically coupled to a high speed integrated photo detector logic gate with a strobable output.

The devices are packaged in an 8-pin small outline package which conforms to the standard SO8 footprint.

Applications

- Ground loop elimination
- LSTTL to TTL, LSTTL or 5 volt CMOS
- Line receiver, data transmission
- Data multiplexing
- Switching power supplies
- Pulse transformer replacement
- Computer peripheral interface

Truth Table (Positive Logic)

Input	Output
H	L
L	H

Absolute Maximum Ratings (Ta=25°C)

Parameter		Symbol	Rating	Unit
Input	DC/ Average Forward current	I _F	20	mA
	Reverse voltage	V _R	5	V
	Power dissipation	P _D	45	mW
Output	Power dissipation	P _C	60	mW
	Output current	I _O	50	mA
	Output voltage	V _O	7.0	V
Supply voltage (max 1 minute)		V _{CC}	7.0	V
Output Power Dissipation		P _O	80	mW
Isolation voltage ^{*1}		V _{ISO}	3750	V rms
Operating temperature		T _{OPR}	-40 ~ +100	°C
Storage temperature		T _{STG}	-55 ~ +125	°C
Soldering temperature ^{*2}		T _{SOL}	260	°C

Notes:

^{*1} AC for 1 minute, R.H.= 40 ~ 60% R.H. In this test, pins 1, 2, 3, 4 are shorted together, and pins 5, 6, 7, 8 are shorted together.

^{*2} For 10 seconds

Electrical Characteristics (Ta=-40 to 85°C unless specified otherwise)**Input**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Forward voltage	V_F	-	1.4	1.8	V	$I_F = 10\text{mA}$
Reverse voltage	V_R	5.0	-	-	V	$I_R = 10\mu\text{A}$
Temperature coefficient of forward voltage	$\Delta V_F/\Delta T_A$	-	-1.8	-	mV/°C	$I_F = 10\text{mA}$
Input capacitance	C_{IN}	-	60	-	pF	$V_F = 0, f = 1\text{MHz}$

Output

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
High level supply current	I_{CCH}	-	13	18	mA	$I_F = 0\text{mA}, V_{CC} = 5.5\text{V}$
Low level supply current	I_{CCL}	-	15	21	mA	$I_F = 10\text{mA}, V_{CC} = 5.5\text{V}$

Transfer Characteristics (Ta=-40 to 85°C unless specified otherwise)

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
HIGH Level Output Current	I_{OH}	-	-	100	μA	$V_{CC} = 5.5\text{V}, V_O = 5.5\text{V}, I_F = 250\mu\text{A}$
LOW Level Output Current	V_{OL}	-	-	0.6	V	$V_{CC} = 5.5\text{V}, I_F = 5\text{mA}, I_{CL} = 13\text{mA}$
Input Threshold Current	I_{FT}	-	-	5	mA	$V_{CC} = 5.5\text{V}, V_O = 0.6\text{V}, I_{OL} = 13\text{mA}$

Switching Characteristics (T_a=-40 to 85°C, V_{CC}=5V, I_F=7.5mA unless specified otherwise)

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
Propagation delay time to output High level ^{*4} (Fig.11)	t _{PHL}	-	-	100	ns	C _L =15pF, R _L =350Ω, T _A =25°C
Propagation delay time to output Low level ^{*5} (Fig.11)	t _{PLH}	-	-	100	ns	C _L =15pF, R _L =350Ω, T _A =25°C
Pulse width distortion	t _{PHL} - t _{PLH}	-	-	35	ns	C _L =15pF, R _L =350Ω
Output rise time ^{*6} (Fig.11)	t _r	-	40	-	ns	C _L =15pF, R _L =350Ω
Output fall time ^{*7} (Fig.11)	t _f	-	10	-	ns	C _L =15pF, R _L =350Ω
Common Mode Transient Immunity at Logic High ^{*8}	EL0630 EL0631	ICM _H I	5000 10000	-	V/μs	I _F =0mA, V _{OH(MIN)} =2.0V, R _L =350Ω, T _A =25°C IV _{CMI} =1KV(Fig.12)
Common Mode Transient Immunity at Logic Low ^{*9}	EL0630 EL0631	ICM _L I	5000 10000	-	V/μs	I _F =7.5mA, V _{OL(MAX)} =0.8V, R _L =350Ω, T _A =25°C IV _{CMI} =1KV(Fig.12)

Typical Electro-Optical Characteristics Curves

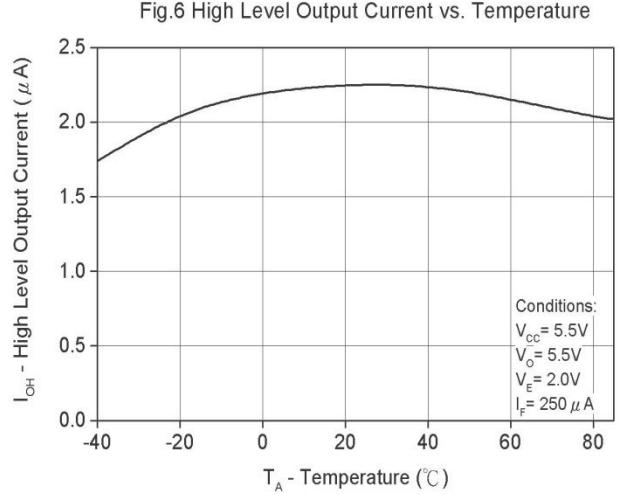
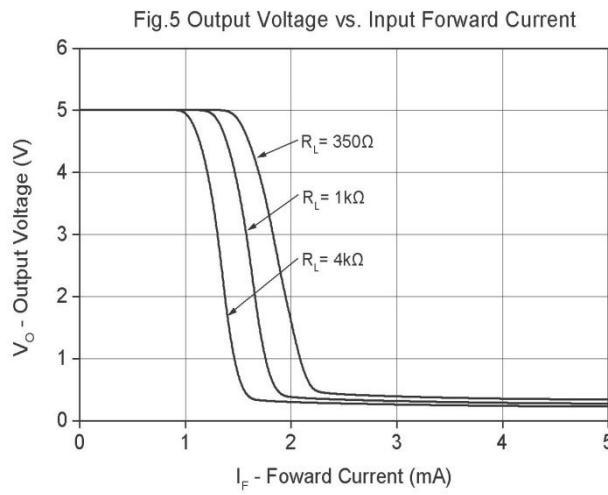
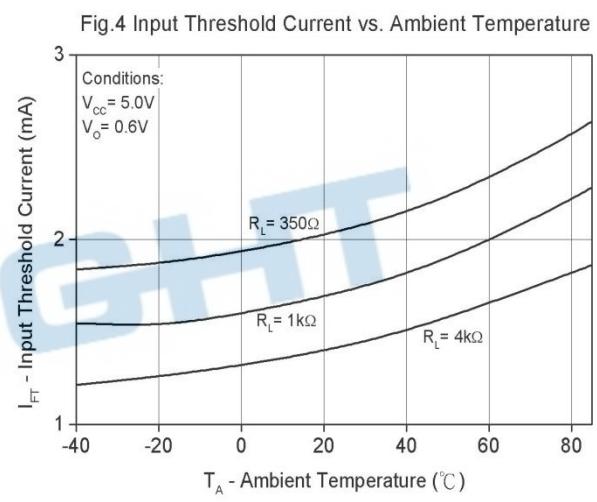
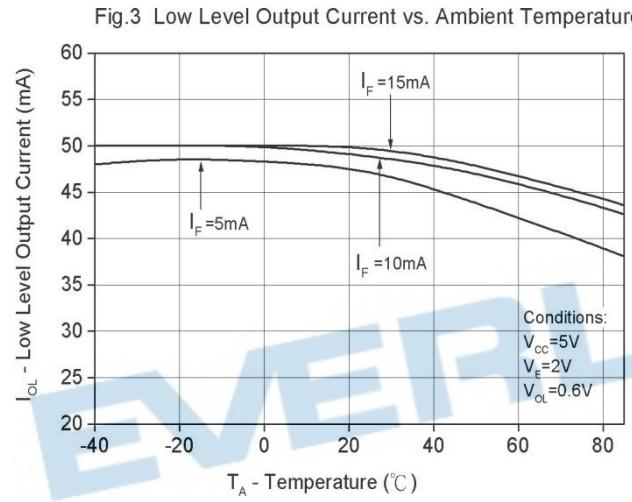
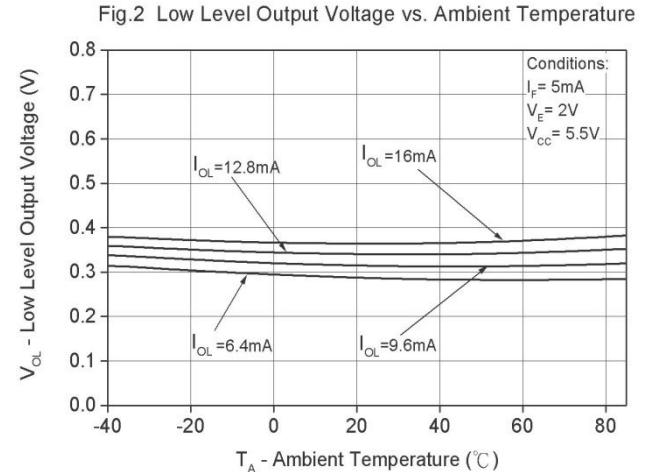
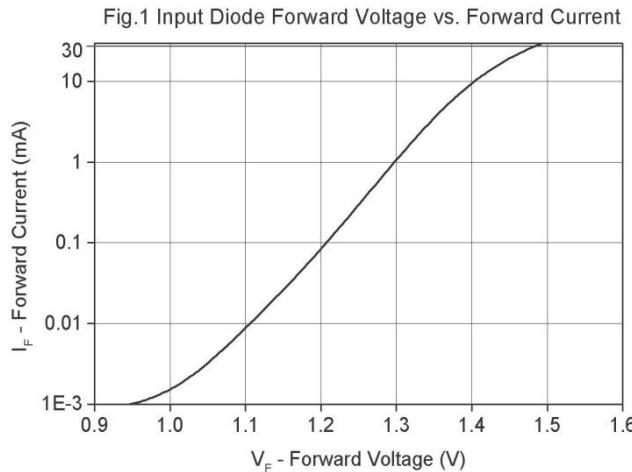


Fig.7 Switching Time vs. Forward Current

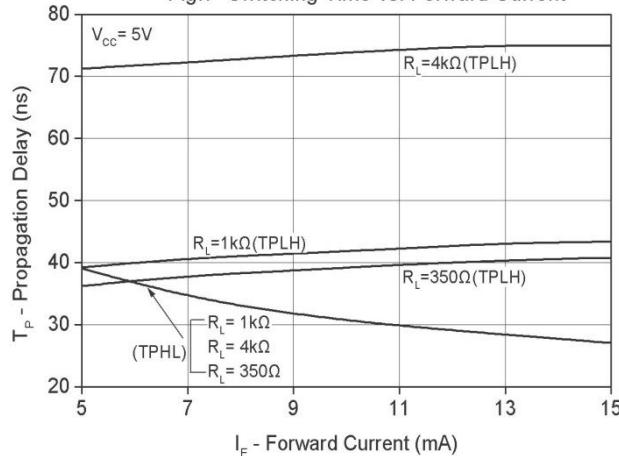


Fig.8 Switching Time vs. Temperature

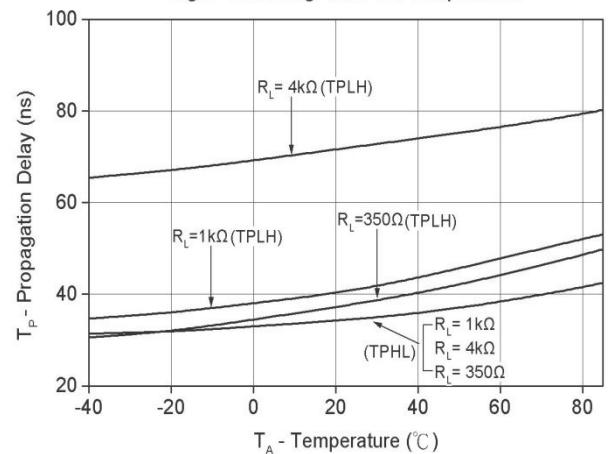


Fig.9 Pulse Width Distortion vs. Temperature

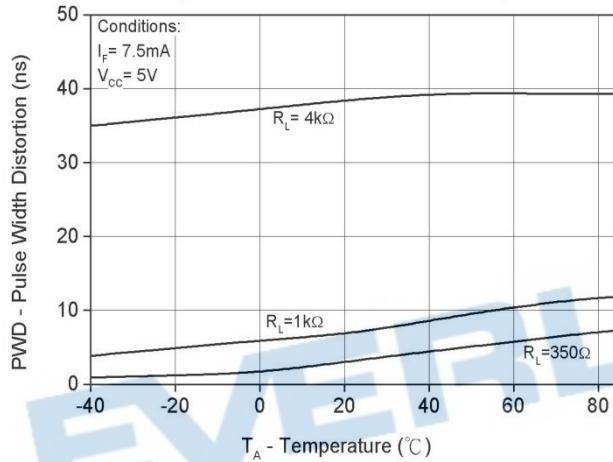


Fig.10 Rise and Fall Time vs. Temperature

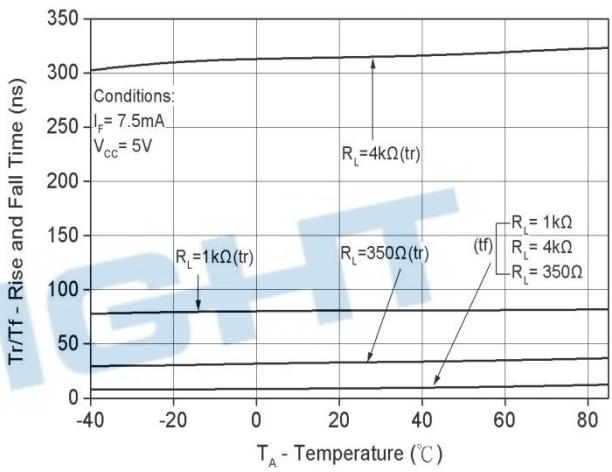


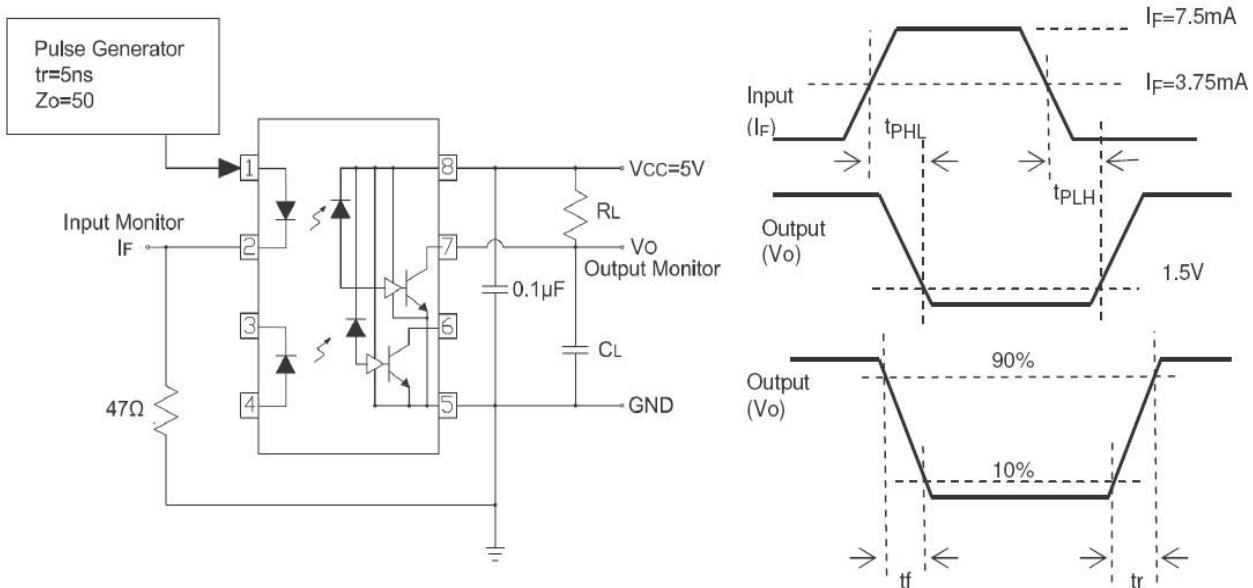
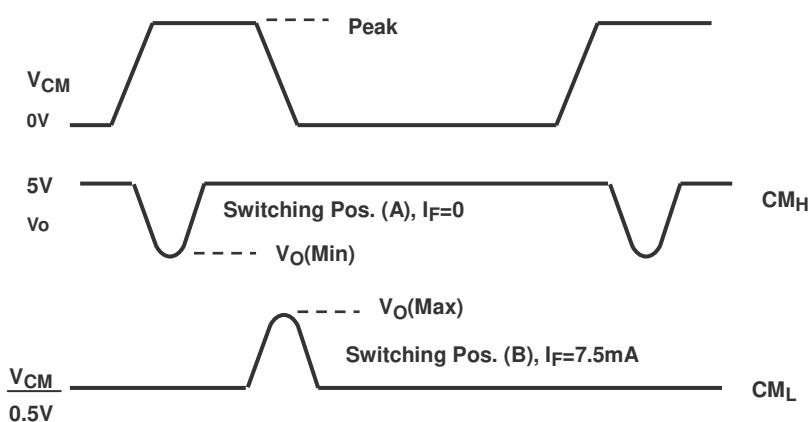
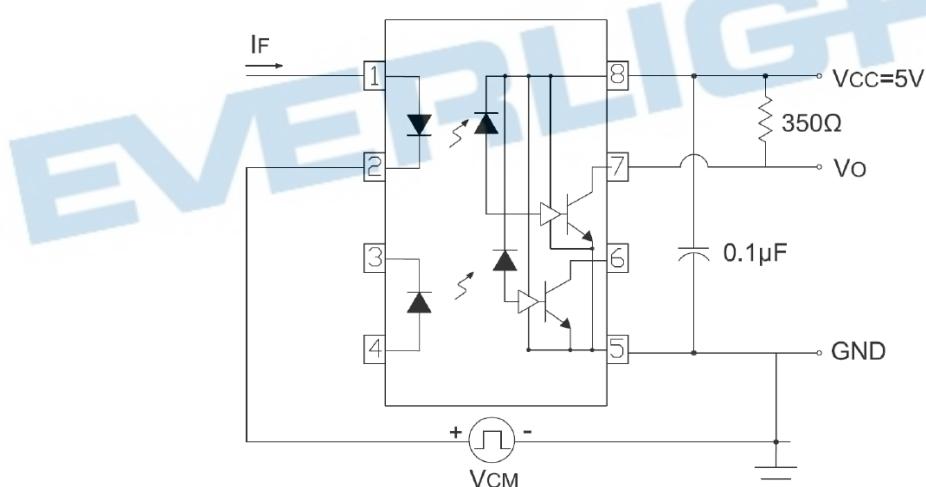
Fig. 11 Test circuit and waveforms for t_{PHL} , t_{PLH} , t_r , and t_f 

Fig. 12 Test circuit Common mode Transient Immunity



Notes

- *3 The V_{CC} supply must be bypassed by a $0.1\mu F$ capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package V_{CC} and GND pins
- *4. t_{PLH} – Propagation delay is measured from the 3.75mA level on the HIGH to LOW transition of the input current pulse to the 1.5 V level on the LOW to HIGH transition of the output voltage pulse.
- *5. t_{PHL} – Propagation delay is measured from the 3.75mA level on the LOW to HIGH transition of the input current pulse to the 1.5 V level on the HIGH to LOW transition of the output voltage pulse.
- *6. t_r – Rise time is measured from the 90% to the 10% levels on the LOW to HIGH transition of the output pulse.
- *7. t_f – Fall time is measured from the 10% to the 90% levels on the HIGH to LOW transition of the output pulse.
- *8 CM_H – The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the HIGH state (i.e., $V_{OUT} > 2.0V$).
- *9 CM_L – The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the LOW output state (i.e., $V_{OUT} < 0.8V$).

Order Information

Part Number

EL063X(Z)-V

Note

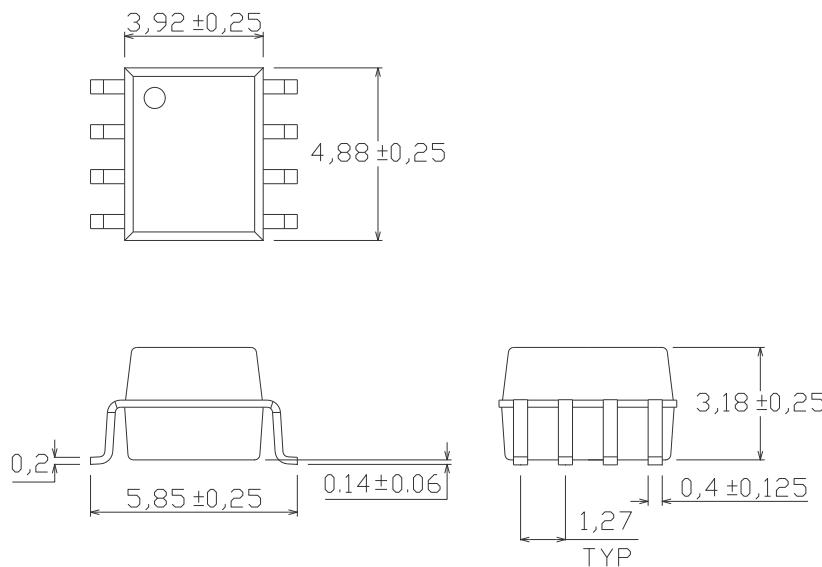
X = Part no. (X = 0 or 1)

Z = Tape and reel option (TA, TB or none).

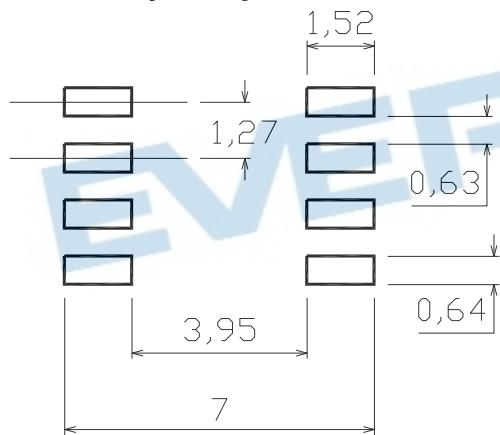
V = VDE (optional)

Option	Description	Packing quantity
None	Standard	100 units per tube
-V	Standard + VDE	100 units per tube
(TA)	TA tape & reel option	2000 units per reel
(TB)	TB tape & reel option	2000 units per reel
(TA)-V	TA tape & reel option + VDE	2000 units per reel
(TB)-V	TB tape & reel option + VDE	2000 units per reel

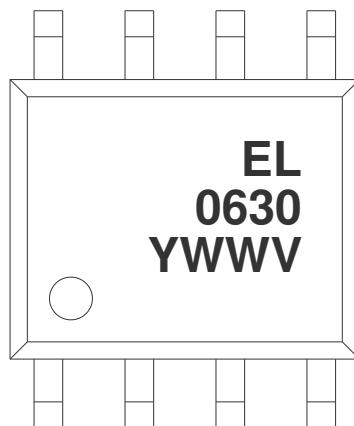
Package Dimension (Dimensions in mm)



Recommended pad layout for surface mount leadform



Device Marking

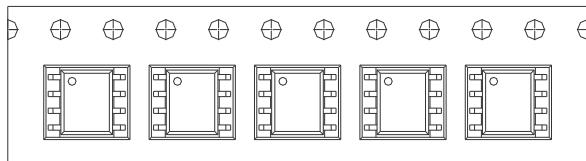
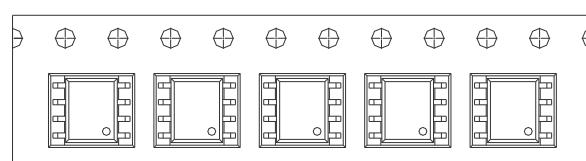


Notes

0630 denotes Device Number
Y denotes 1 digit Year code
WW denotes 2 digit Week code
V denotes VDE (optional)

EVERLIGHT

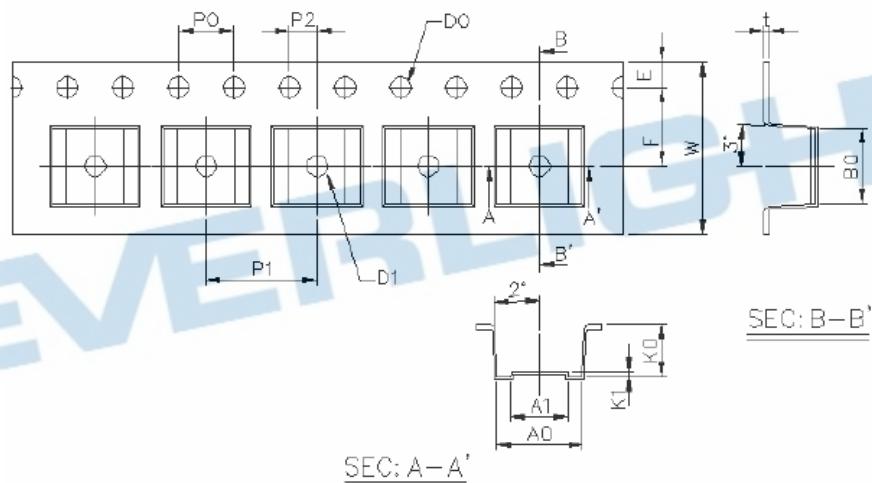
Tape & Reel Packing Specifications

Option TAOption TB

Direction of feed from reel

Direction of feed from reel

Tape dimensions

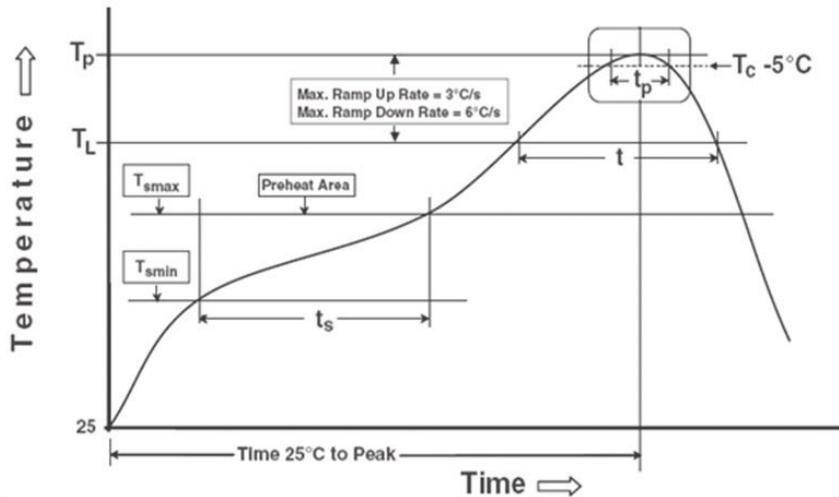


Dimension No.	A0	A1	B0	D0	D1	E	F
Dimension(mm)	6.2 ± 0.1	4.1 ± 0.1	5.28 ± 0.1	1.5 ± 0.1	1.5 ± 0.3	1.75 ± 0.1	5.5 ± 0.1
Dimension No.	P0	P1	P2	t	W	K0	K1
Dimension(mm)	4.0 ± 0.1	8.0 ± 0.1	2.0 ± 0.1	0.4 ± 0.1	$12.0 +0.3/-0.1$	3.7 ± 0.1	0.3 ± 0.1

Precautions for Use

1. Soldering Condition

1.1 (A) Maximum Body Case Temperature Profile for evaluation of Reflow Profile



Note:

Reference: IPC/JEDEC J-STD-020D

Preheat

Temperature min (T_{smin})

150 °C

Temperature max (T_{smax})

200°C

Time (T_{smin} to T_{smax}) (t_s)

60-120 seconds

Average ramp-up rate (T_{smax} to T_p)

3 °C/second max

Other

Liquidus Temperature (T_L)

217 °C

Time above Liquidus Temperature (t_L)

60-100 sec

Peak Temperature (T_p)

260°C

Time within 5 °C of Actual Peak Temperature: $T_p - 5^\circ\text{C}$

30 s

Ramp- Down Rate from Peak Temperature

6°C /second max.

Time 25°C to peak temperature

8 minutes max.

Reflow times

3 times

DISCLAIMER

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2. When using this product, please observe the absolute maximum ratings and the instructions for using outlined in these specification sheets. EVERLIGHT assumes no responsibility for any damage resulting from use of the product which does not comply with the absolute maximum ratings and the instructions included in these specification sheets.
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A large, faint, light blue watermark of the word "EVERLIGHT" in a bold, sans-serif font. The text is oriented diagonally, sloping upwards from the bottom-left to the top-right. The letters are slightly transparent, allowing the background content to be visible through them.