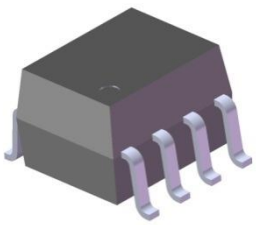
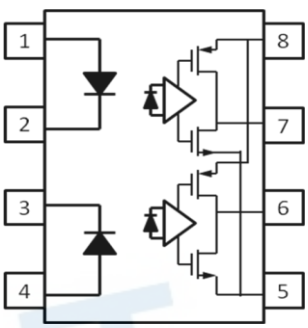
EVERLIGHT

DATASHEET

8 PIN SOP 3.3V DUAL CHANNEL HIGH SPEED 15MBit/s LOGIC GATE PHOTOCOUPLER EL083L EL086L Series



Schematic



Pin Configuration

1, Anode
2, Cathode
3, Cathode
4, Anode
5, Gnd
6, Vout2
7, Vout1
8, V_{CC}

Features

- •Compliance Halogen Free
  (Br <900 ppm ,Cl <900 ppm , Br+Cl < 1500 ppm)
- 3.3 and 5 V CMOS compability
- High speed 15Mbit/s
- 10kV/μs min. common mode transient immunity(EL086L)
- Guaranteed performance from -40 to 85℃
- Logic gate output, Fan out 10
- High isolation voltage between input and output (Viso=3750 V rms)
- Compliance with EU REACH
- Pb free and RoHS compliant
- UL and cUL approved
- VDE approved
- SEMKO approved
- NEMKO approved
- DEMKO approved
- FIMKO approved

Description

The EL08XL consists of an infrared emitting diode optically coupled to a CMOS detector ICs.

It is packaged in a 8-pin SOP package and is suitable for surface mounting technology.

Applications

- Line receiver, data transmission
- Data multiplexing
- Switching power supplies
- Pulse transformer replacement
- Computer peripheral interface
- High speed logic ground isolation

Truth Table (Positive Logic)

Input	Output
H	L
L	H

Absolute Maximum Ratings (T_A=25℃)

Parameter		Symbol	Rating	Unit
Input	Forward current	I_F	20	mA
	Reverse voltage	V_R	5	V
	Power dissipation	P_D	35	mW
Output	Power dissipation	P_C	85	mW
	Output current	I_O	20	mA
	Output voltage	V_O	5.5	V
	Supply voltage	V_{CC}	5.5	V
Output Power Dissipation		P_O	85	mW
Isolation voltage *2		V_{ISO}	3750	V rms
Operating temperature		T_{OPR}	-40 ~ +85	°C
Storage temperature		T_{STG}	-55 ~ +125	°C
Soldering temperature *3		T_{SOL}	260	°C

Notes:

*1 The V_{CC} supply must be bypassed by a 0.1μF capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package V_{CC} and GND pins.

*2 AC for 1 minute, R.H.= 40 ~ 60% R.H. In this test, pins 1, 2, 3 & 4 are shorted together, and pins 5, 6, 7 & 8 are shorted together.

*3 For 10 seconds

Electrical Characteristics (T_A=-40 to 85°C unless specified otherwise)

Input

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Forward voltage	V_F	-	1.4	1.8	V	I_F = 8mA
Reverse voltage	V_R	5.0	-	-	V	I_R = 10μA
Temperature coefficient of forward voltage	$\Delta V_F/\Delta T_A$	-	-1.8	-	mV/°C	I_F =14mA
Input capacitance	C_{IN}	-	60	-	pF	V_F=0, f=1MHz

Output

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
High level supply current	I_{CCH}	-	2.5	8	mA	I_F=0mA
Low level supply current	I_{CCL}	-	2.5	8	mA	I_F=8mA
High level output voltage	V_{OH}	V_{CC}-1	V_{CC}-0.3	-	V	V_{CC}=3.3V,I_F=0mA, I_O=-4mA
		V_{CC}-1	V_{CC}-0.2	-	V	V_{CC}=5V,I_F=0mA, I_O=-4mA
Low level output voltage	V_{OL}	-	0.21	0.6	V	V_{CC} = 3.3V, I_F=8mA, I_O=4mA
			0.17	0.6	V	V_{CC} = 5.0V, I_F=8mA, I_O=4mA
Input threshold current	I_{FT}	-	2.5	5	mA	I_{OL}=20uA

Switching Characteristics (T_A=-40 to 85°C, V_{CC}=3.3V, I_F=8mA unless specified otherwise)

Parameter		Symbol	Min	Typ.	Max.	Unit	Condition
Propagation delay time to output high level		t_{PHL}	-	38	60	ns	I_F=8mA ,C_L = 15pF, V_{CC}=3.3V CMOS Signal Levels
			-	35	60	ns	I_F=8mA ,C_L = 15pF, V_{CC}=5V CMOS Signal Levels
Propagation delay time to output low level		t_{PLH}	-	41	60	ns	I_F=8mA ,C_L = 15pF, V_{CC}=3.3V CMOS Signal Levels
				46	60	ns	I_F=8mA ,C_L = 15pF, V_{CC}=5V CMOS Signal Levels
Pulse width distortion		$\|t_{PHL} - t_{PLH}\|$	0	6	30	ns	I_F=8mA ,C_L = 15pF, V_{CC}=3.3V CMOS Signal Levels
			0	8	30	ns	I_F=8mA ,C_L = 15pF, V_{CC}=5V CMOS Signal Levels
Output rise time		t_r	-	5.5	-	ns	I_F=8mA ,C_L = 15pF, V_{CC}=3.3V CMOS Signal Levels
Output fall time		t_f	-	6	-	ns	I_F=8mA ,C_L = 15pF, V_{CC}=3.3V CMOS Signal Levels
Common mode transient Immunity at logic high*4	083L	$\|CM_H\|$	5,000	-	-	V/μS	I_F = 0mA , T_A=25°C V_{CM}=1000Vp-p
	086L		10,000			V/μS	I_F = 0mA , T_A=25°C V_{CM}=1000Vp-p
Common mode transient immunity at logic low*5	083L	$\|CM_L\|$	5,000	-	-	V/μS	I_F = 8mA , T_A=25°C V_{CM}=1000Vp-p
	086L		10,000			V/μS	I_F = 8mA , T_A=25°C V_{CM}=1000Vp-p

Typical Electro-Optical Characteristics Curves

Figure 1. Forward Current vs. Forward Voltage

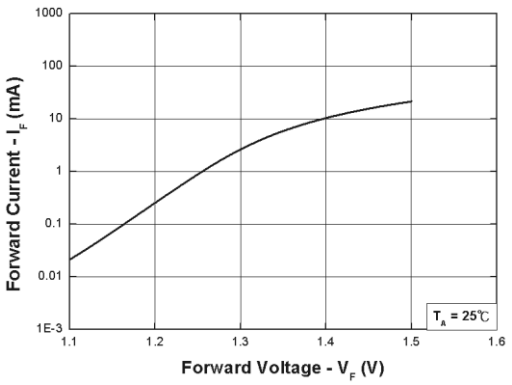


Figure 2. Input Threshold Current vs. Ambient Temperature

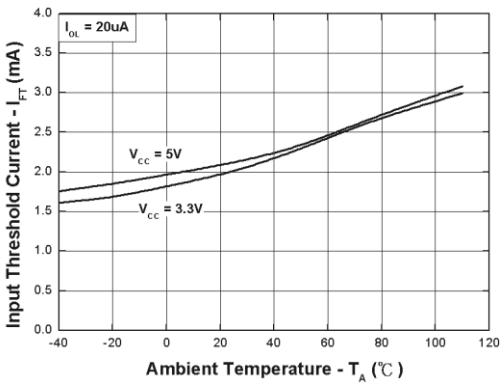


Figure 3. High Level Supply Current vs. Ambient Temperature

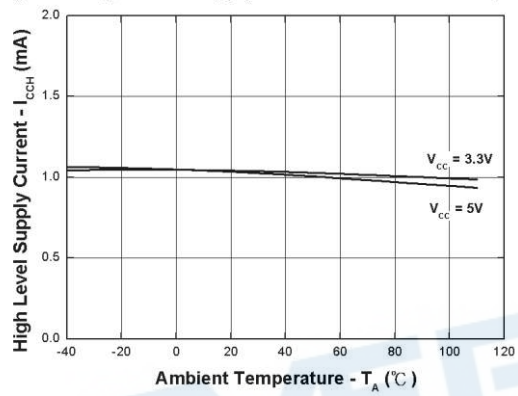


Figure 4. Low Level Supply Current vs. Ambient Temperature

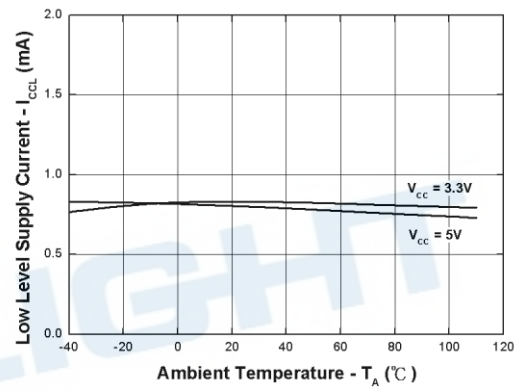


Figure 5. Switching Time vs. Forward Current

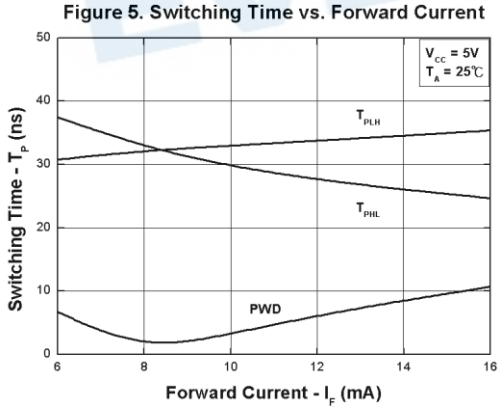


Figure 6. Switching Time vs. Forward Current

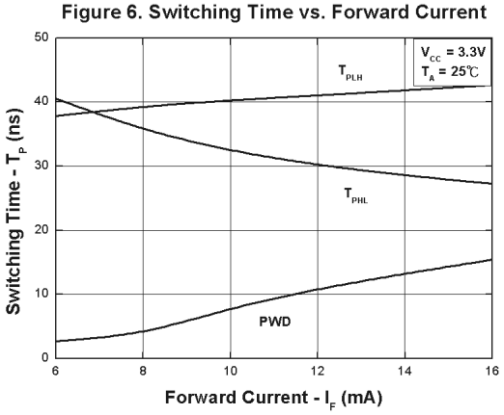


Figure 7. Forward voltage vs. Ambient Temperature

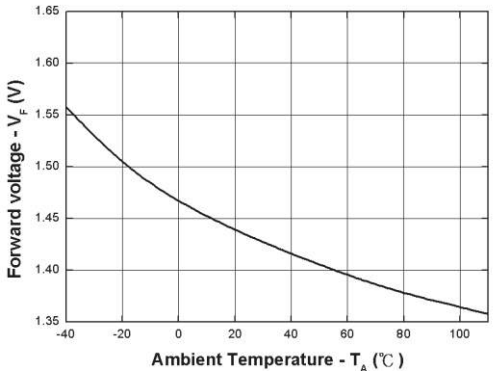


Fig. 8 Test circuit and waveforms for t_{PHL}, t_{PLH}, t_r, and t_f

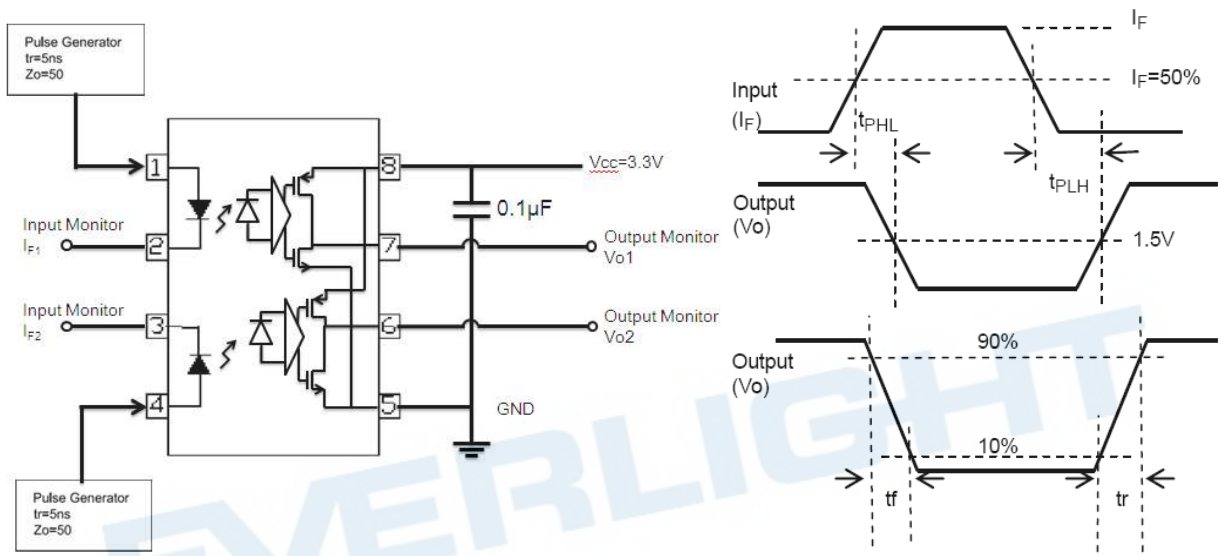
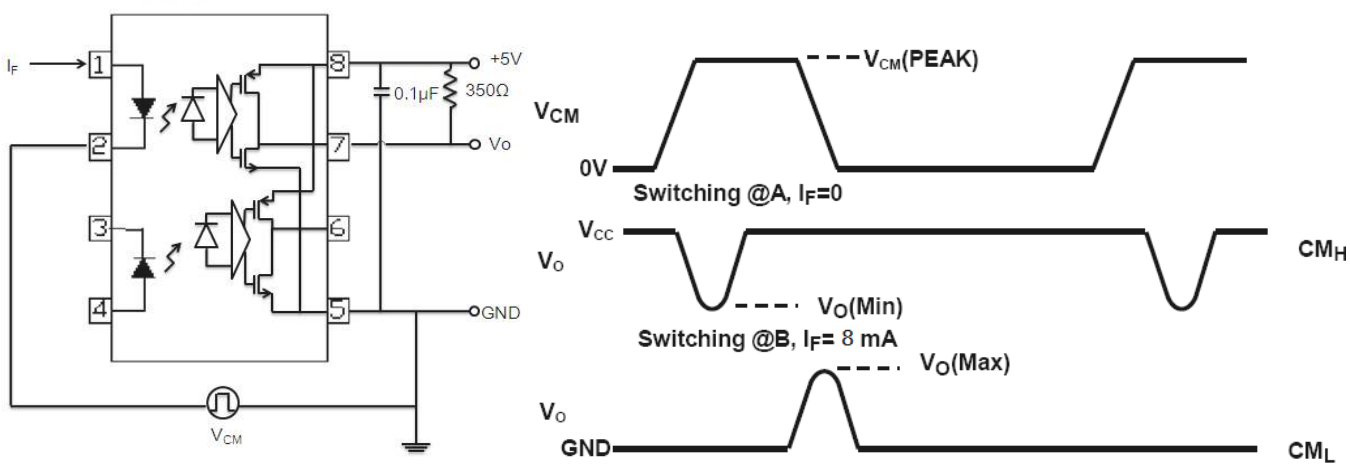


Fig. 9 Test circuit Common mode Transient Immunity



Note

*4. CM_H– The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the HIGH state (i.e., V_{OUT} > 2.0V).

*5. CM_L– The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the LOW output state (i.e., V_{OUT} < 0.8V).

Order Information

Part Number

EL08XL(Z)-V

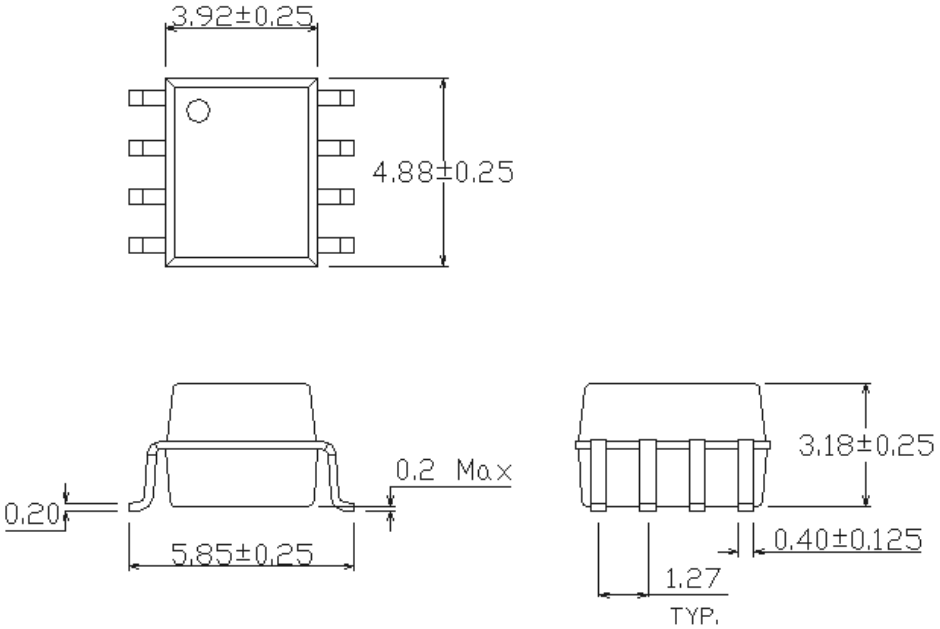
Note

08XL = Part No
Z = Tape and reel option (TA, TB).
V = VDE (optional)

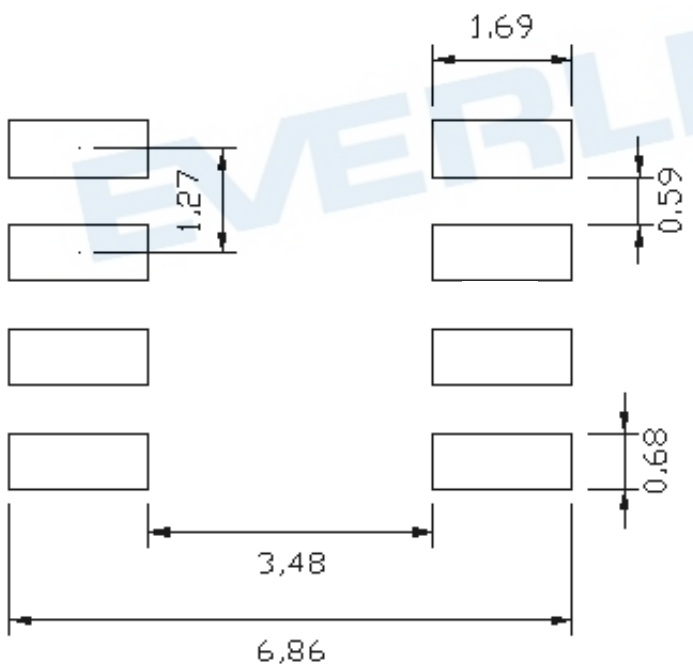
Option	Description	Packing quantity
(TA)	TA tape & reel option	2000 units per reel
(TB)	TB tape & reel option	2000 units per reel
(TA)-V	TA tape & reel option + VDE	2000 units per reel
(TB)-V	TB tape & reel option + VDE	2000 units per reel

Package Dimension

(Dimensions in mm)



Recommended pad layout for surface mount leadform



Notes

Suggested pad dimension is just for reference only.
Please modify the pad dimension based on individual need.

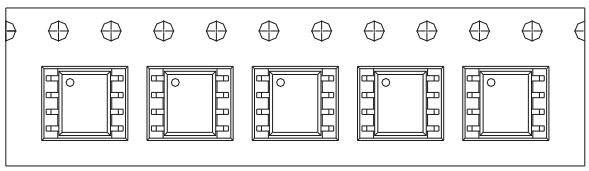
Device Marking

Notes

EL	denotes EVERLIGHT
083L	denotes Device Number
Y	denotes 1 digit Year code
WW	denotes 2 digit Week code
V	denotes VDE (optional)

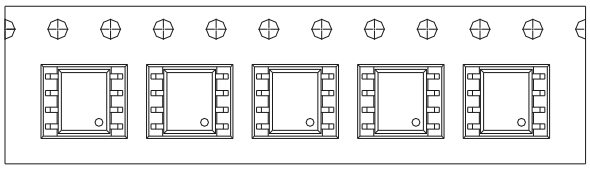
Tape & Reel Packing Specifications

Option TA



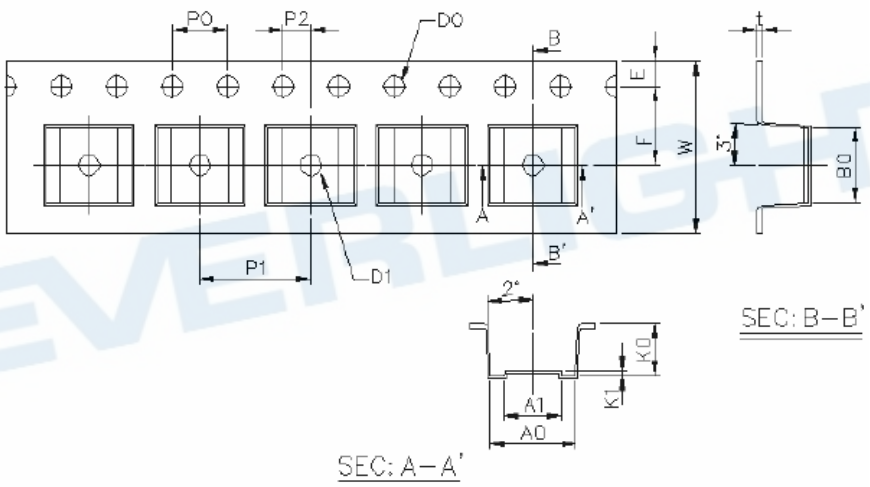
Direction of feed from reel

Option TB



Direction of feed from reel

Tape dimension

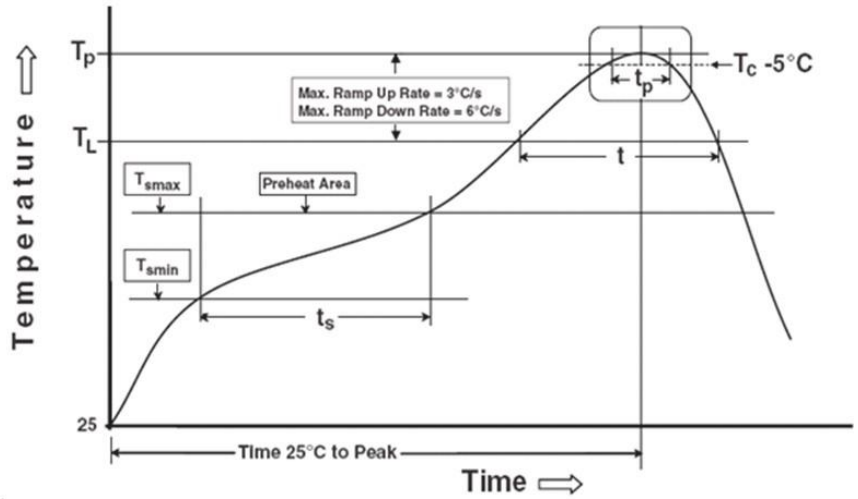


Dimension No.	A0	A1	B0	D0	D1	E	F
Dimension(mm)	6.2±0.1	4.1±0.1	5.28±0.1	1.5±0.1	1.5±0.3	1.75±0.1	5.5±0.1
Dimension No.	**Po**	**P1**	**P2**	**t**	**W**	**K0**	**K1**
Dimension(mm)	4.0±0.1	8.0±0.1	2.0±0.1	0.4±0.1	12.0+0.3/ -0.1	3.7±0.1	0.3±0.1

Precautions for Use

1. Soldering Condition

1.1 (A) Maximum Body Case Temperature Profile for evaluation of Reflow Profile



Note: Reference: IPC/JEDEC J-STD-020D

Preheat	
Temperature min (T_{smin})	150 °C
Temperature max (T_{smax})	200°C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max
Other	
Liquidus Temperature (T_L)	217 °C
Time above Liquidus Temperature (t_L)	60-100 sec
Peak Temperature (T_P)	260°C
Time within 5 °C of Actual Peak Temperature: T_P - 5°C	30 s
Ramp- Down Rate from Peak Temperature	6°C /second max.
Time 25°C to peak temperature	8 minutes max.
Reflow times	3 times

Disclaimer

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