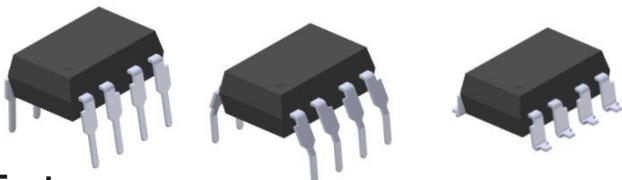


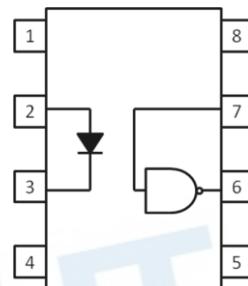
8 PIN DIP 3.3V HIGH SPEED - 10MBit/s LOGIC GATE PHOTOCOUPLED EL260L



Features

- 3.3 and 5 V dual supply voltage
- High speed 10Mbit/s
- 10kV/μs min. common mode transient immunity
- Guaranteed performance from -40 to 85°C
- Logic gate output, Fan out 10
- High isolation voltage between input and output ($V_{iso}=5000$ V rms)
- Pb free and RoHS compliant.
- UL and cUL approved(No. E214129)
- VDE approved (No. 132249)
- SEMKO approved
- NEMKO approved
- DEMKO approved
- FIMKO approved
- CQC approved

Schematic



A 0.1μF bypass capacitor must be connected between pins 8 and 5 *1

Pin Configuration

- 1, No Connection
- 2, Anode
- 3, Cathode
- 4, No Connection
- 5, Gnd
- 6, V_{out}
- 7, V_E
- 8, V_{cc}

Description

The EL260L is consists of an infrared emitting diode optically coupled to a high speed integrated photo detector logic gate with a strobable output. It is packaged in a 8-pin DIP package and available in wide-lead spacing and SMD options.

Applications

- Ground loop elimination
- LSTTL to TTL, LSTTL or 5 volt CMOS
- Line receiver, data transmission
- Data multiplexing
- Switching power supplies
- Pulse transformer replacement
- Computer peripheral interface
- High speed logic ground isolation

Truth Table (Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H
H	NC	L
L	NC	H

Absolute Maximum Ratings (T_A=25°C)

	Parameter	Symbol	Rating	Unit
Input	Forward current	I _F	50	mA
	Enable input voltage Not exceed V _{CC} by more than 500mV	V _E	V _{CC} + 0.5	V
	Enable Input Current	I _E	5	mA
	Reverse voltage	V _R	5	V
Output	Power dissipation	P _D	45	mW
	Power dissipation	P _C	85	mW
	Output current	I _O	50	mA
	Output voltage	V _O	7.0	V
	Supply voltage	V _{CC}	7.0	V
	Output Power Dissipation	P _O	85	mW
	Isolation voltage ^{*2}	V _{ISO}	5000	V rms
	Operating temperature	T _{OPR}	-40 ~ +85	°C
	Storage temperature	T _{STG}	-55 ~ +125	°C
	Soldering temperature ^{*3}	T _{SOL}	260	°C

Notes:

^{*1} The V_{CC} supply must be bypassed by a 0.1μF capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package V_{CC} and GND pins

^{*2} AC for 1 minute, R.H.= 40 ~ 60% R.H. In this test, pins 1, 2, 3 & 4 are shorted together, and pins 5, 6, 7 & 8 are shorted together.

^{*3} For 10 seconds

Electrical Characteristics ($T_A=-40$ to 85°C unless specified otherwise)

Input

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Forward voltage	V_F	-	1.4	1.8	V	$I_F = 10\text{mA}$
Reverse voltage	V_R	5.0	-	-	V	$I_R = 10\mu\text{A}$
Temperature coefficient of forward voltage	$\Delta V_F/\Delta T_A$	-	-1.8	-	$\text{mV}/^\circ\text{C}$	$I_F = 10\text{mA}$
Input capacitance	C_{IN}	-	60	-	pF	$V_F=0, f=1\text{MHz}$

Output

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
High level supply current	I_{CCH}	-	7	10	mA	$I_F=0\text{mA}, V_E=0.5\text{V}, V_{CC}=3.3\text{V}$
Low level supply current	I_{CCL}	-	9	13	mA	$I_F=10\text{mA}, V_E=0.5\text{V}, V_{CC}=3.3\text{V}$
High level enable current	I_{EH}	-	-	-1.6	mA	$V_E=2.0\text{ V}, V_{CC}=3.3\text{V}$
Low level enable current	I_{EL}	-	-	-1.6	mA	$V_E=0.5\text{ V}, V_{CC}=3.3\text{V}$
High level enable voltage	V_{EH}	2.0	-	-	V	$I_F=10\text{mA}, V_{CC}=3.3\text{V}$
Low level enable voltage ^{*4}	V_{EL}	-	-	0.8	V	$I_F=10\text{mA}, V_{CC}=3.3\text{V}$

Transfer Characteristics ($T_A=-40$ to 85°C unless specified otherwise)

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
High level output current	I_{OH}	-	5.0	100	μA	$V_{CC}=3.3\text{V}, V_O=3.3\text{V}, I_F=250\mu\text{A}, V_E=2.0\text{V}$
Low level output current	V_{OL}	-	0.35	0.6	V	$V_{CC} = 3.3\text{V}, I_F=5\text{mA}, V_E=2.0\text{V}, I_{OL}=13\text{mA}$
Input threshold current	I_{FT}	-	2.5	5	mA	$V_{CC} = 3.3\text{V}, V_O=0.6\text{V}, V_E = 2.0\text{V}, I_{OL}=13\text{mA}$

Switching Characteristics (T_A=-40 to 85°C, V_{CC}=3.3V, I_F=7.5mA unless specified otherwise)

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
Propagation delay time to output high level ^{*5} (Fig.12)	t _{PHL}	-	40	75	ns	C _L = 15pF, R _L =350Ω, T _A =25°C
Propagation delay time to output low level ^{*6} (Fig.12)	t _{PLH}	-	45	75	ns	C _L = 15pF, R _L =350Ω, T _A =25°C
Pulse width distortion	t _{PHL} - t _{PLH}	-	5	35	ns	C _L = 15pF, R _L =350Ω
Output rise time ^{*7} (Fig.12)	t _r	-	40	-	ns	C _L = 15pF, R _L =350Ω
Output fall time ^{*8} (Fig.12)	t _f	-	10	-	ns	C _L = 15pF, R _L =350Ω
Enable propagation delay time to output High Level ^{*9} (Fig.13)	t _{EHL}	-	25	-	ns	I _F = 7.5mA , V _{EH} =3.0V, C _L = 15pF, R _L =350Ω
Enable propagation delay time to output low level ^{*10} (Fig.13)	t _{EHL}	-	10	-	ns	I _F = 7.5mA , V _{EH} =3.0V, C _L = 15pF, R _L =350Ω
Common mode transient immunity at logic high ^{*11}	CM _H	10,000	-	-	V/μS	I _F = 7.5mA , V _{OH} =2.0V, R _L =350Ω, T _A =25°C V _{CM} =400Vp-p (Fig.14)
Common mode transient immunity at logic low ^{*12}	CM _L	10,000	-	-	V/μS	I _F = 0mA , V _{OL} =0.8V, R _L =350Ω, T _A =25°C V _{CM} =400Vp-p (Fig.14)

Typical Electro-Optical Characteristics Curves

Figure 1. Forward Current vs Forward Voltage

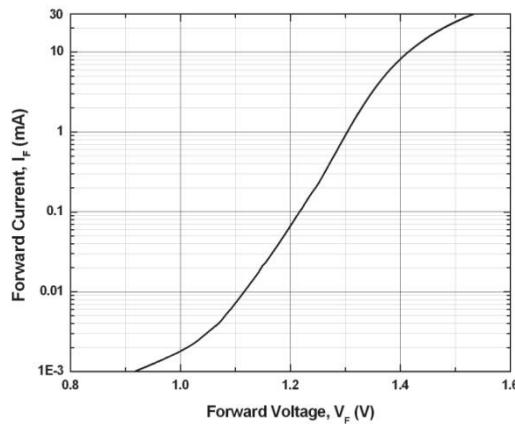


Figure 2. Low Level Output Voltage vs Ambient Temperature

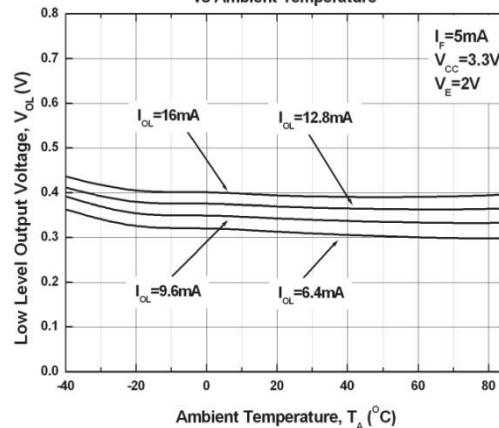


Figure 3. Low Level Output Current vs Ambient Temperature

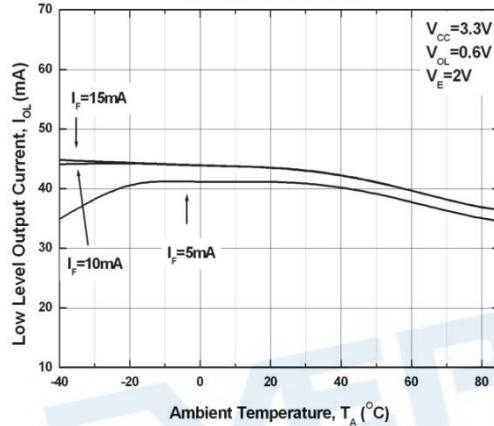


Figure 4. Input Threshold Current vs Ambient Temperature

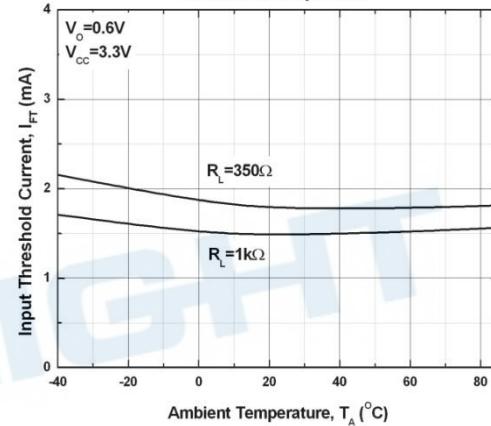


Figure 5. Input Current vs Output Voltage

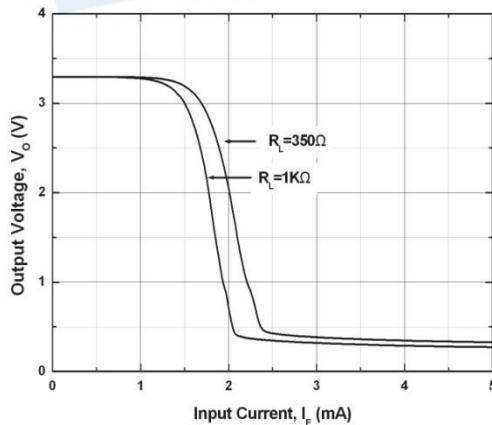


Figure 6. High Level Output Current vs Ambient Temperature

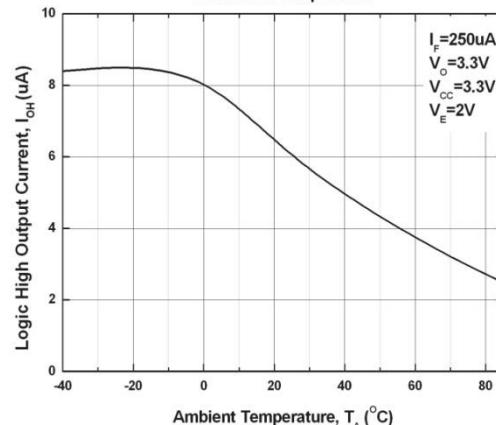


Figure 7. Propagation Delay vs. Forward Current

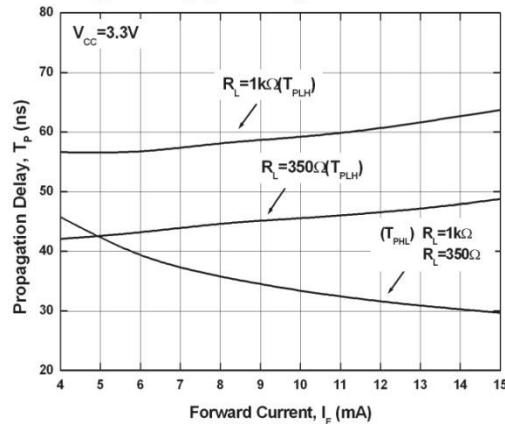


Figure 8. Propagation Delay vs. Temperature

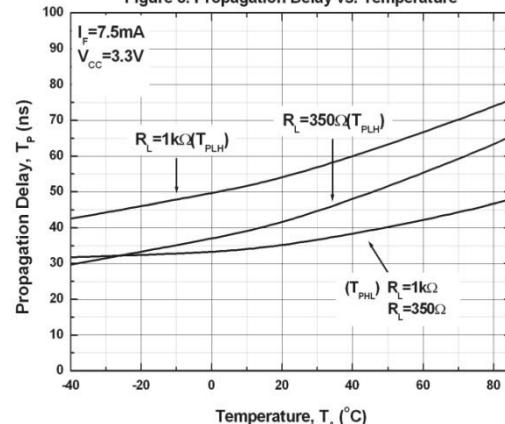


Figure 9. Pulse Width Distortion vs. Temperature

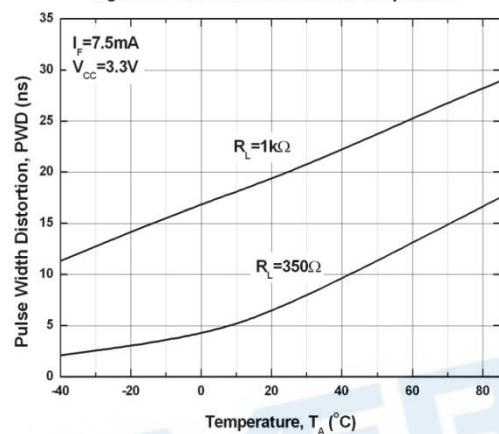


Figure 10. Rise and Fall Time vs. Temperature

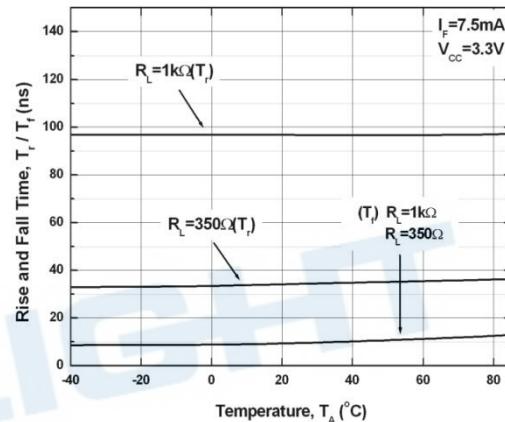


Figure 11. Enable Propagation Delay vs. Temperature

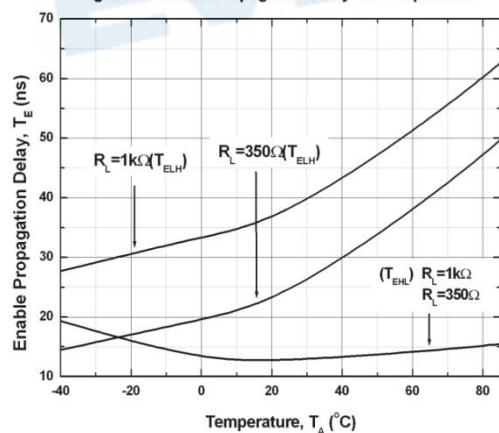


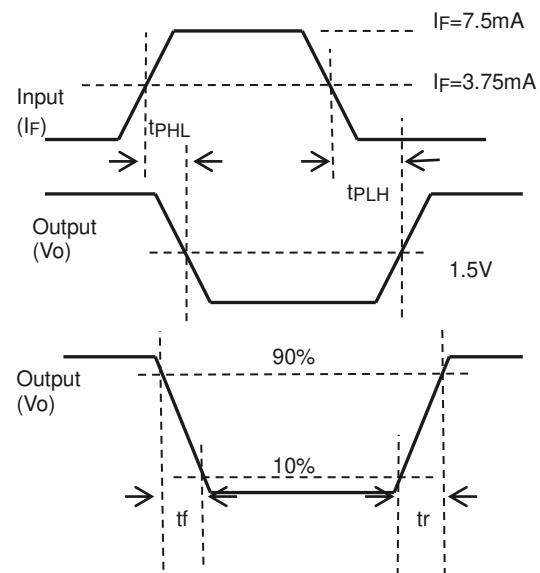
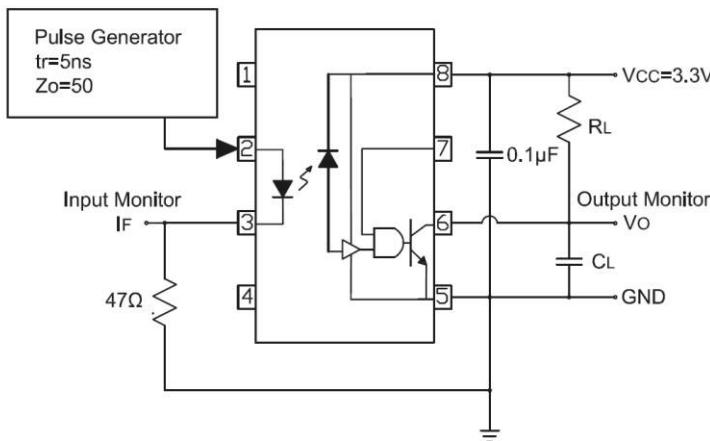
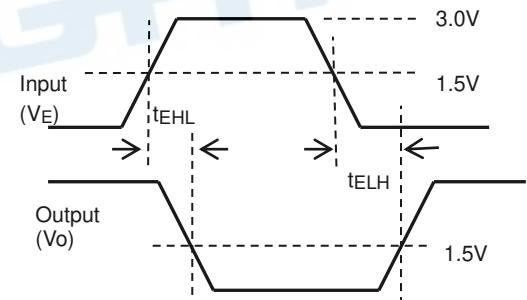
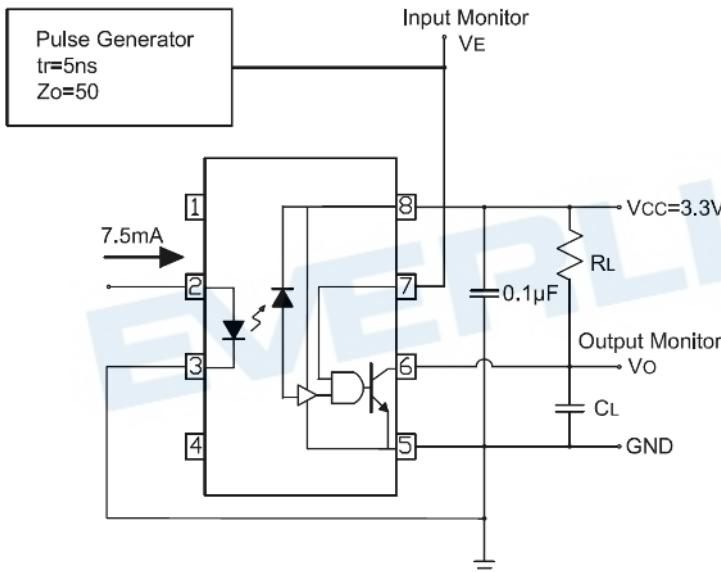
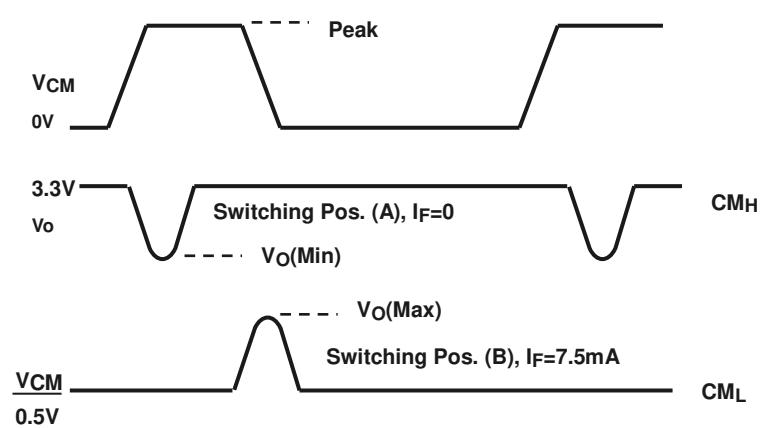
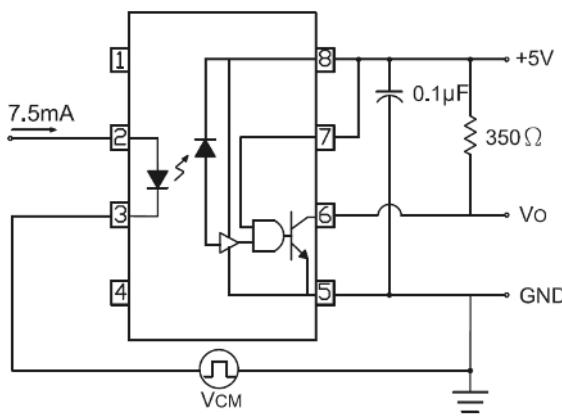
Fig. 12 Test circuit and waveforms for t_{PHL} , t_{PLH} , t_r , and t_f Fig. 13 Test circuit and waveform for t_{EHL} and t_{ELH} 

Fig. 14 Test circuit Common mode Transient Immunity



Note

- *4. Enable Input – No pull up resistor required as the device has an internal pull up resistor.
- *5. t_{PLH} – Propagation delay is measured from the 3.75mA level on the HIGH to LOW transition of the input current pulse to the 1.5 V level on the LOW to HIGH transition of the output voltage pulse.
- *6. t_{PHL} – Propagation delay is measured from the 3.75mA level on the LOW to HIGH transition of the input current pulse to the 1.5 V level on the HIGH to LOW transition of the output voltage pulse.
- *7. t_r – Rise time is measured from the 90% to the 10% levels on the LOW to HIGH transition of the output pulse.
- *8. t_f – Fall time is measured from the 10% to the 90% levels on the HIGH to LOW transition of the output pulse.
- *9. t_{ELH} – Enable input propagation delay is measured from the 1.5V level on the HIGH to LOW transition of the input voltage pulse to the 1.5V level on the LOW to HIGH transition of the output voltage pulse.
- *10. t_{EHL} – Enable input propagation delay is measured from the 1.5V level on the LOW to HIGH transition of the input voltage pulse to the 1.5V level on the HIGH to LOW transition of the output voltage pulse.
- *11 CM_H – The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the HIGH state (i.e., V_{OUT} > 2.0V).
- *12 CM_L – The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the LOW output state (i.e., V_{OUT} < 0.8V).

A large, faint watermark of the word "EVERLIGHT" in a bold, sans-serif font, oriented diagonally from the bottom-left towards the top-right of the page.

Order Information

Part Number

EL260LY(Z)-V

Note

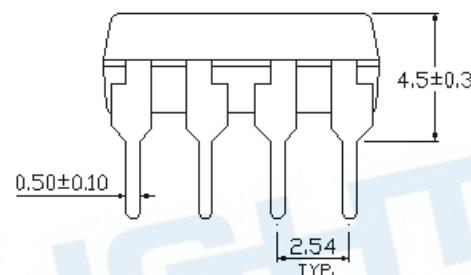
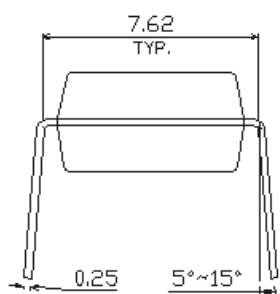
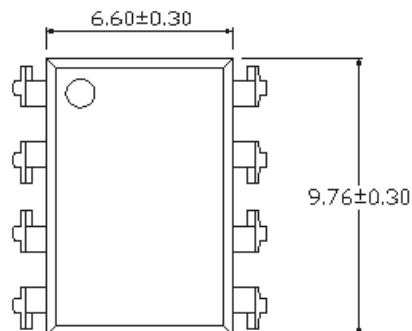
Y = Lead form option (S, S1, M or none)
Z = Tape and reel option (TA, TB or none).
V = VDE (optional)

Option	Description	Packing quantity
None	Standard DIP-8	45 units per tube
M	Wide lead bend (0.4 inch spacing)	45 units per tube
S (TA)	Surface mount lead form + TA tape & reel option	1000 units per reel
S (TB)	Surface mount lead form + TB tape & reel option	1000 units per reel
S1 (TA)	Surface mount lead form (low profile) + TA tape & reel option	1000 units per reel
S1 (TB)	Surface mount lead form (low profile) + TB tape & reel option	1000 units per reel

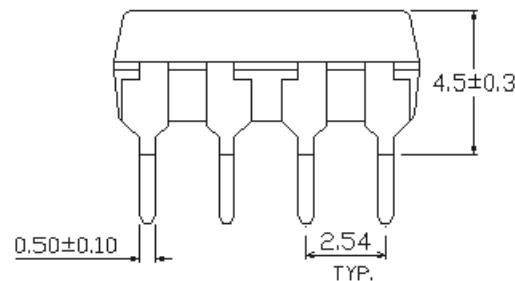
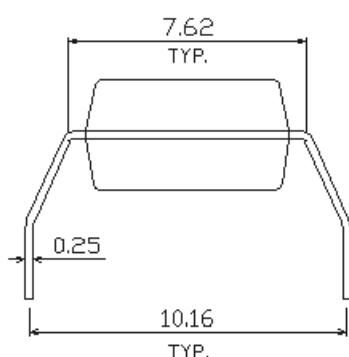
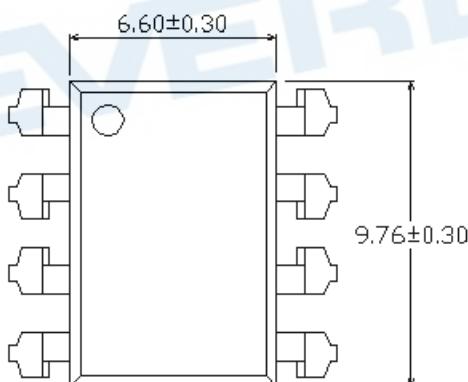
Package Dimension

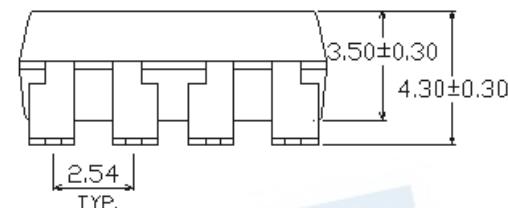
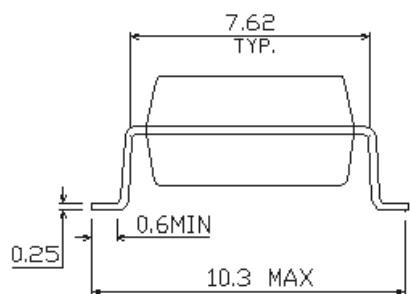
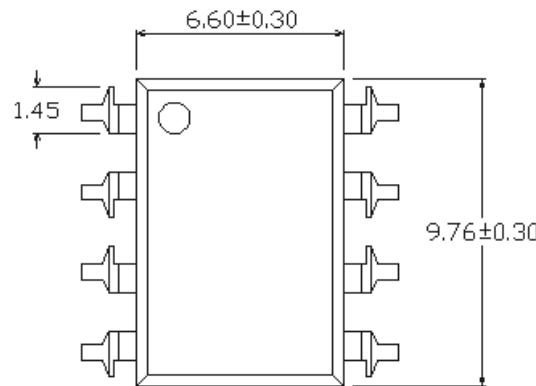
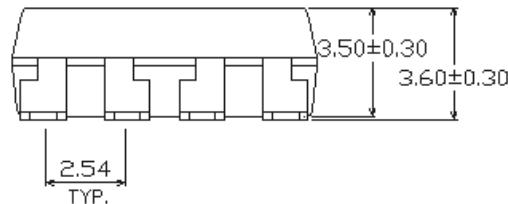
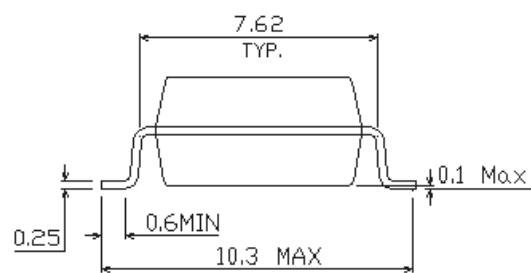
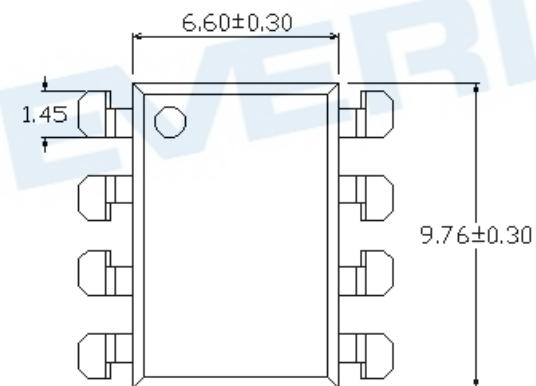
(Dimensions in mm)

Standard DIP Type

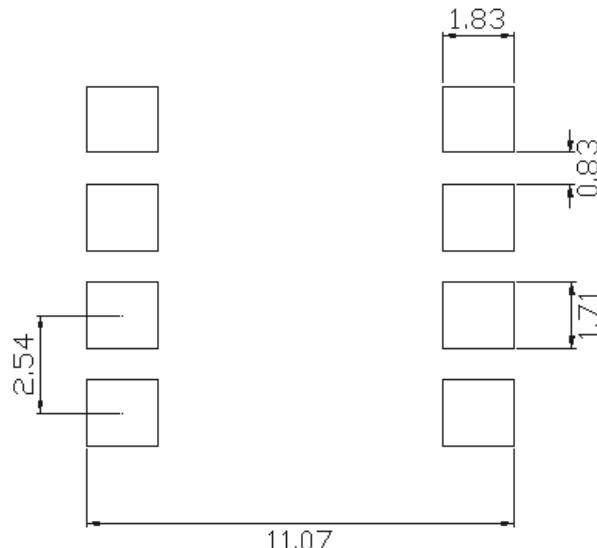


Option M Type



Option S Type**Option S1 Type**

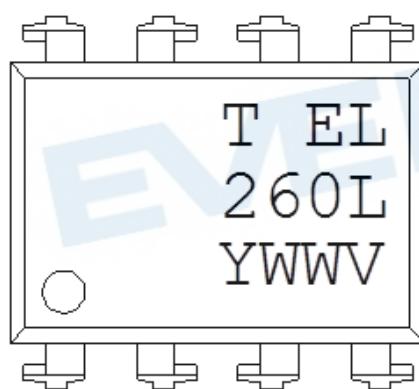
Recommended pad layout for surface mount leadform



Notes.

Suggested pad dimension is just for reference only.
Please modify the pad dimension based on individual need.

Device Marking

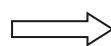
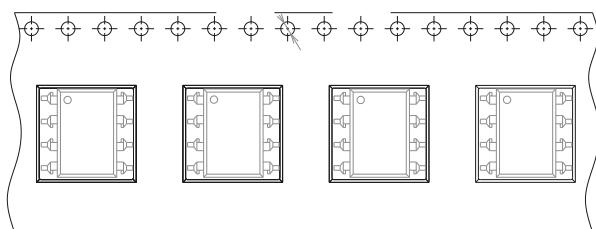


Notes

T	denotes Factory No code : made in China T : made in Taiwan
EL	denotes EVERLIGHT
260L	denotes Device Number
Y	denotes 1 digit Year code
WW	denotes 2 digit Week code
V	denotes VDE (optional)

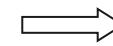
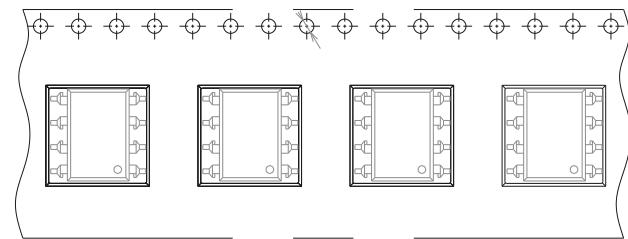
Tape & Reel Packing Specifications

Option TA



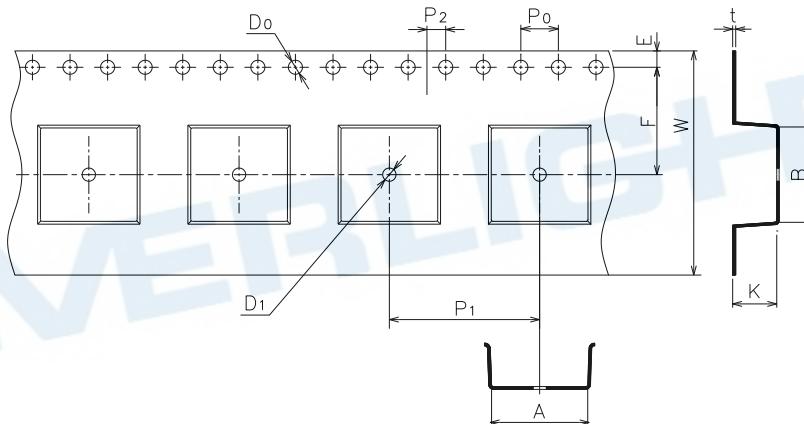
Direction of feed from reel

Option TB



Direction of feed from reel

Tape dimension

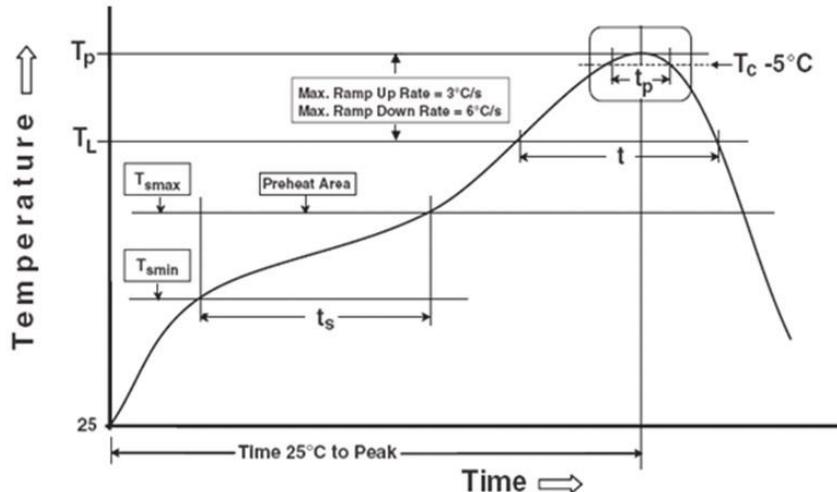


Dimension No.	A	B	Do	D1	E	F
Dimension (mm)	10.4 ± 0.1	10.0 ± 0.1	$1.5 +0.1/-0$	1.5 ± 0.25	1.75 ± 0.1	7.5 ± 0.1
Dimension No.	Po	P1	P2	t	W	K
Dimension (mm)	4.0 ± 0.1	12.0 ± 0.1	2.0 ± 0.05	0.4 ± 0.05	16.0 ± 0.3	4.5 ± 0.1

Precautions for Use

1. Soldering Condition

1.1 (A) Maximum Body Case Temperature Profile for evaluation of Reflow Profile



Note:

Reference: IPC/JEDEC J-STD-020D

Preheat

Temperature min (T_{smin})	150 °C
Temperature max (T_{smax})	200°C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max

Other

Liquidus Temperature (T_L)	217 °C
Time above Liquidus Temperature (t_L)	60-100 sec
Peak Temperature (T_p)	260°C
Time within 5 °C of Actual Peak Temperature: $T_p - 5^\circ\text{C}$	30 s
Ramp- Down Rate from Peak Temperature	6°C /second max.
Time 25°C to peak temperature	8 minutes max.
Reflow times	3 times

Disclaimer

1. Above specification may be changed without notice. EVERLIGHT will reserve authority on material change for above specification.
2. The graphs shown in this datasheet are representing typical data only and do not show guaranteed values.
3. When using this product, please observe the absolute maximum ratings and the instructions for use outlined in these specification sheets. EVERLIGHT assumes no responsibility for any damage resulting from use of the product which does not comply with the absolute maximum ratings and the instructions included in these specification sheets.
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